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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,743	01/27/2004	Samson S. Wong	SUNMP382	2837

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EXAMINER
CHASE, SHELLY A

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
	10/766,743	WONG ET AL.
Office Action Summary	Examiner	Art Unit	
	Shelly A. Chase	2133	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>*27 January 2004*</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7 and 11-17* is/are rejected.

7)☒ Claim(s) *3-6 and 8-10* is/are objected to.

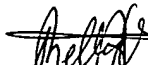8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

SHELLY CHASE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date <u>2-28-2005</u>.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1 to 17 are presented for examination.

Information Disclosure Statement

2.   The references listed in the information disclosure statement submitted on 2-28-

2005 have been considered by the examiner (see attached PTO-1449).

Drawings

3.   The drawings are objected to because the drawings as filed do not comply with
the drawing requirements set forth in the MPEP.

Claim Objections

4.   Claims 5 and 15 are objected to because of the following informalities: please

change the dependency to correct the seemingly antecedent basis errors for instance

claim 5 should depend on claim 2. [1]

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

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[1] Note: For compact prosecution it is assumed that claim 5 is dependent on claim 2 and claim 15 is
dependent on claim 12.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6.   Claims **1, 2, 7, 11** to **13, 15** and **16** are rejected under 35 U.S.C. 102(b) as being anticipated by Saxena et al. (WO 96/42053).

Claim **1**:

Saxena teaches the claimed invention. Saxena teaches a method and an apparatus for detecting memory address errors, the method comprising: a parity generator (115) generating parity addresses (117) ("generating a first parity address") (see fig. 1 and pg. 6 lines 5 to 10) and exclusive OR gates (122 & 124) encoding the address parity bit into two bits (120) of the Hamming code by hashing ("scrambling at least two data error –correction-code (ECC) check bits using the first parity address") (see pg. 6 lines 10 to 24). Saxena also teaches that hamming codes are error detection and correction codes (see pg. 4, lines 1 to 3). Saxena further teaches that the encoded bits are stored in memory (see pg. 6, lines 25 to 28).

As per claim **2**, Saxena teaches a parity generator (208) generates parity for an address that is read ("generating a second address parity using the memory address") (see fig. 2 and pg. 6, lines 30 to 35). Saxena also teaches that data and hamming codes bits are read from the memory and two XOR gates (216 & 218) are used to produce a error code wherein the error code is an unhashed error code ("unscrambling the at least two data ECC check bits using the second address parity") (see pg. 7, lines 5 to 15 and pg. 8 lines 1 et seq.). Saxena further teaches the hamming code is used to check for address errors (see pg. 8, lines 10 to 15).

Claim **7**:

Saxena teaches the claimed invention. Saxena teaches a method and an

apparatus for detecting memory address errors, the method comprising: a parity

generator (208) generating parity for an address that is read from a memory

("generating a second address parity using the memory address") (see fig. 2 and pg. 6,

lines 30 to 35). Saxena also teaches that data and hamming codes bits are read from

the memory and two XOR gates (216 & 218) are used to produce a error code wherein

the error code is an unhashed error code ("unscrambling the at least two data ECC

check bits using the second address parity") (see pg. 7, lines 5 to 15 and pg. 8 lines 1 et

seq.). Saxena further teaches the hamming code is used to check for address errors

(see pg. 8, lines 10 to 15).

Claim **11**:

. Saxena teaches the claimed invention. Saxena teaches a method and an

apparatus for detecting memory address errors, the method comprising: a parity

generator (115) generating parity addresses (117) from an address at input (104)

("generating a first parity address") (see fig. 1 and pg. 6 lines 5 to 10). Saxena also

teaches that the parity generator is coupled to two exclusive OR gates (122 & 124) that

encodes the address parity bit into two bits (120) of the Hamming code ("scrambling at

least two data error –correction-code (ECC) check bits using the first parity address").

(see pg. 6 lines 10 to 24). Saxena further teaches that for double bit error detection and

single bit error correction the XOR gates of figure 1 are used (see pg. 6, lines 20 et

seq.).

As per claim **12**, Saxena teaches a parity generator (208) generates parity for an

address that is read ("generating a second address parity using the memory address")

(see fig. 2 and pg. 6, lines 30 to 35). Saxena also teaches that data and hamming

codes bits are read from the memory and two XOR gates (216 & 218) are used to

produce a error code wherein the error code is an unhashed error code ("unscrambling

the at least two data ECC check bits using the second address parity") (see pg. 7, lines

5 to 15 and pg. 8 lines 1 et seq.). Saxena further teaches the hamming code is used to

check for address errors (see pg. 8, lines 10 to 15).

As per claims **13, 15** and **16**, Saxena teaches that the parity generators and XOR

gates are all part of a device ("memory controller") and are coupled to a memory device

(138 or 234) through address input (104 or 208) and data lines (102 and 220, 222 &

228) (see fig. 1-2 and pg. 6, lines 1 et seq.).

Claim Rejections - 35 USC § 103

7.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

8.   Claims **14** and **17** are rejected under 35 U.S.C. 103(a) as being unpatentable

over Saxena et al. in view of Borkenhagen et al. (USP 6754858 B2).

As per claims **14** and **17**, Saxena does not specifically teach that the memory controller is coupled to a central processing unit (CPU) core and that memory is selected from a group consisting of a static random access memory and a dynamic random access memory; however, Borkenhagen in an analogous art teaches a synchronous dynamic random access memory (SDRAM) address error detection method and apparatus comprising a computer (100) with a memory controller (104) connected to a processor (102) and multiple SDRAM (see fig. 1). Borkenhagen also teaches that in computer systems memory read data originates in a DRAM (see col. 1, lines 63 to 65) and an address error detection can be performed for a DRAM or a SDRAM (see col. 5, lines 5 to 13).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus for detecting memory address of Saxena such that the memory controller is coupled to a processor and that address error detection can be performed for a DRAM or a SDRAM as taught by Borkenhagen since, Borkenhagen teaches the system provides an effective mechanism for detecting and correcting address errors (see col. 2, lines 20 et seq.). This modification would have been obvious because a person of ordinary skill in the art would have been motivated to employ a device capable of detecting and correcting multiple bit errors as taught by Borkenhagen.
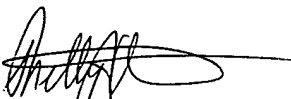
Allowable Subject Matter

9.   Claims 3 to 6 and 8 to 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A. Chase whose telephone number is 571-272-3816. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SHELLY CHASE
PRIMARY EXAMINER